

**LIST OF PRIOR ART CITED BY
APPLICANT**

(PTO-1449)

ATTY. DOCKET NO.
INTEL-0059

APPLN. SERIAL NO.
NEW 10/748,300

APPLICANT(S)
KyeHyung LEE et al.

FILING DATE
December 31, 2003

GROUP
2816

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	*PATENT NO.	*ISSUE DATE	*INVENTOR NAME	CLASS	SUBCLASS	FILING DATE
W	6,351,191	02/26/02	Nair et al.	331	57	

U.S. PATENT APPLICATION PUBLICATIONS

	*PATENT APPLN. PUB. NO.	*PUB. DATE	*APPLICANT	CLASS	SUBCLASS	

U.S. PATENT APPLICATIONS

	*APPLN. NO.	*FILING DATE	*INVENTOR	CLASS	SUBCLASS	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Publisher, Place of Publication, Etc.)

W	Noda et al. "AN ON-CHIP TIMING ADJUSTER WITH SUB-100-PS RESOLUTION FOR A HIGH-SPEED DRAM INTERFACE," 1998 Symposium on VLSI Circuits Digest of Technical Papers, pages 62-63
W	John G. Maneatis "LOW-JITTER PROCESS-INDEPENDENT DLL AND PLL BASED ON SELF-BIASED TECHNIQUES," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pages 1723-1732

EXAMINER

DATE CONSIDERED

02/09/2005